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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS

In Re:	Robert Varney	
Serial No:	10/003,982	Group: 2825
Filed:	October 30, 2001	Examiner: Dimyan
For:	Scan Diagnosis System & Method	

August 27, 2004

MAILING CERTIFICATE

I, Lance M. Kreisman, Registration No. 39,256, certify that this correspondence was placed in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria VA 22313-1450, and I have a reasonable basis to believe that it will be deposited with the U.S. Postal Service as first class mail, postage prepaid, on or before August 27, 2004.

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Commissioner for Patents
P.O. Box 1450
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APPLICANT'S BRIEF

Pursuant to 37 CFR 1.192, the Applicants respectfully submit the following Appeal Brief in support of the patentability of Claims 24-27, 32-35 and 37-44 of the subject application.

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I. Real Party in Interest

The real party in interest with respect to the subject matter of this appeal, by virtue of an assignment executed on 10/29/2001 and filed with the Patent and Trademark Office on 10/30/2001, is Teradyne, Inc., 321 Harrison Avenue, Boston, MA 02118.

II. Related Appeals and Interferences

The Applicants assert that there are no known appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status Of the Claims

Claims 24-27, 32-35 and 37-44 are pending and stand rejected in the application. Claims 1-23, 28-31, 26-36 and 45-54 have been cancelled.

IV. Status of Any Amendments

An amendment was filed on June 22, 2004 following the Final Office Action dated March 22, 2004 to address trivial matters noted in the Final Office Action. The Amendment was entered by the Examiner.

V. Summary of the Invention

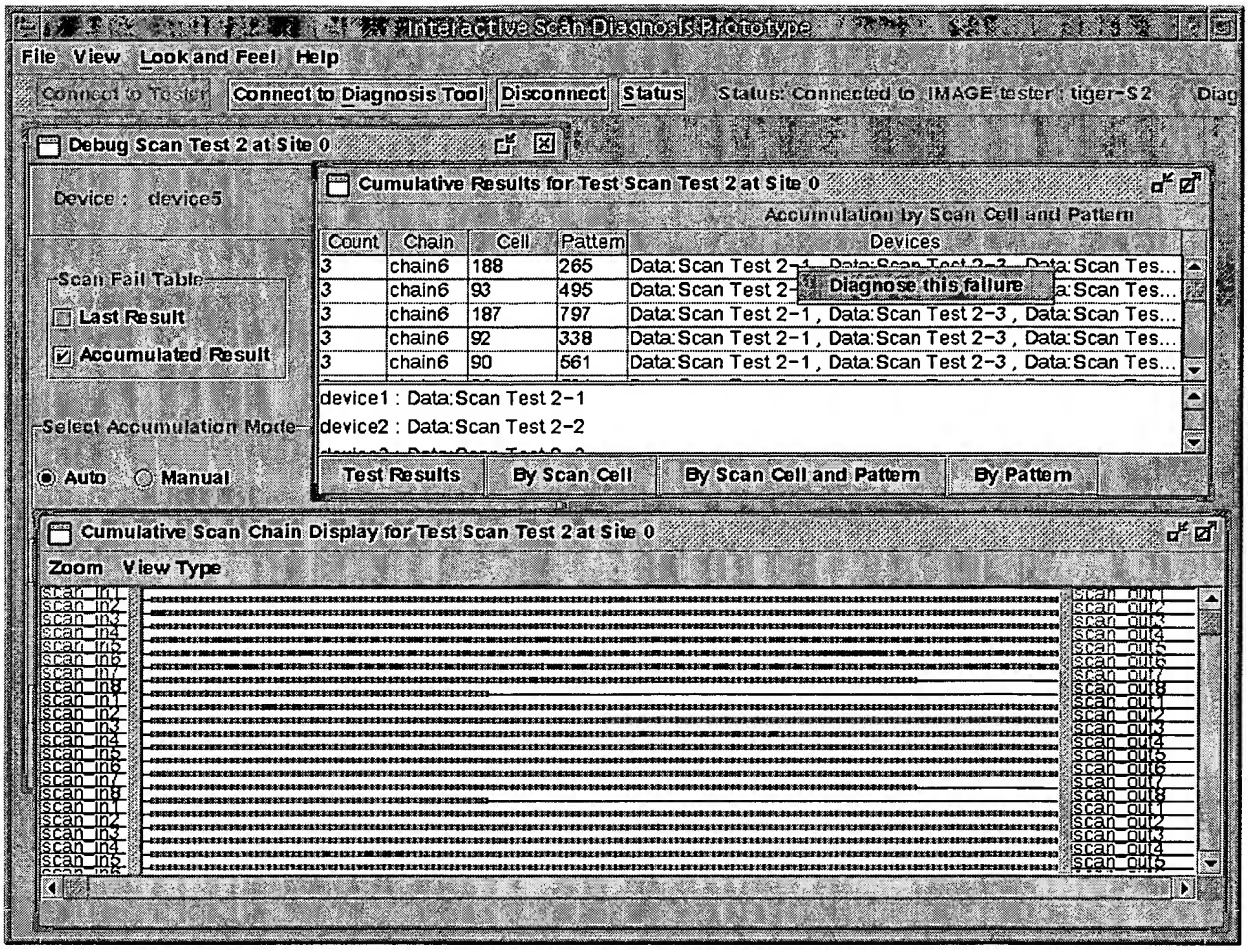
The invention relates to semiconductor testers used in the manufacture of semiconductor devices and in particular provides advantages in processing and evaluating scan chain failure data.

Automatic test equipment is often divided into two categories - functional test and structural (or design-for-test, DFT). Functional test provides the ability to run the device under a variety of real-world operating conditions (Page 1, lines 10 - 19). DFT test, on the other hand, provides limited test capability that looks more to whether the device has any manufacturing defects (Page 1, lines 19 - 24). The limited capability of DFT testing correlates to reduced test costs for some manufacturers.

In order to take advantage of DFT testing, chip designers typically include a series of interconnected flip-flop cells, known in the art as "scan chains" (Page 1, lines 25 - 34). Testing the scan chains involves serially shifting data through the cells, and determining whether the correct outputs show up at the last scan cell (Page 1, lines 28 - 33). Conventionally, scan chain failure information is often tabulated in a list format, noting the identification of the scan chain, and it's relative location in the chip. Shown below is what is believed to be a portion of a tabulated list of scan chain failure data from U.S. Patent No. 6,185,707 to Smith et al., and further discussed herein. The tabulated information may then be used for a subsequent diagnosis process to further determine the cause of the failures.

```
DeviceID = DEMOID
LotID = TESTLOT01
WaferID = 01
DIE = -4.0
datalog.scan.10 diagnosis summary, #failing_patterns=9  #defects=2
#unexplained_fails=2
unexplained patterns = 212 250
-------------------------------------------------------------------
fault candidates for defect 1,  #failing_patterns_explained=5
-------------------------------------------------------------------
Warning: Fault candidates will cause passing patterns to fail.
failing patterns explained = 322 706 738 770
type    code    pin_pathname
----    ----    ------------------------------------
  1     DS      /XTIO_0/XTTLI8_1612/N2_23
  1     DS      /PI9
-------------------------------------------------------------------
diagnosis CPU time = .68 sec
```

FIG._3
(PRIOR ART)



While viewing a list of failed scan chain information such as that shown in Smith is within the realm of possibility, the reality is that manufacturers often test hundreds of devices simultaneously, or within a short period of time. Moreover, each scan chain is often tested hundreds of times during a single pass. Failure data from the myriad of devices and test passes is often not readily comprehensible in a tabulated list format.

With these problems in mind, the scan diagnosis system and method defined in the claims on appeal provides a graphical user interface (GUI) generator 60 (Figure 1) to condense failed scan chain data into a file that is then used to generate graphical representations of the scan chains. An example from Figure 8 of the instant application is shown above. The lower rectangular area illustrates graphical representations of scan chains. This significantly improves the presentability of the data into a format that is readily comprehensible to a test engineer.

VI. The Issues on Appeal

1. Whether claims 24-27, 32-35 and 37-44 are unpatentable under 35 USC §103(a) as obvious over Smith et al. (U.S. Patent No. 6,185,707) in view of Testa et al. (U.S. Patent No. 5,845,234)

VII. Applicants Groupings of Claims

Group I - Claims 24 - 27, 32 - 35
Group II - Claims 37 - 44

Each group of claims listed above is patentable over the others. The groups of claims therefore do not stand or fall together.

125 **VIII. Arguments Asserted By Applicants**

1. Claims 24 - 27, 32 - 35, and 37-44 are not Rendered Obvious by Smith in View of Testa.

The teachings of Smith describe a mapping scheme to facilitate pinpoint physical x-y defect locations of failing transistors on an integrated circuit. As part of his process, Smith utilizes failed scan chain data in the form of a tabulated list which is translated to help generate the physical X-Y data in the form of netlist nodes. The nodes are then bitmapped to facilitate the construction of a visual display of the physical X-Y defect locations.

An important aspect of the Smith disclosure is the omission of any motivation to use the list of failed scan chains by itself, much less take on the additional effort to display a graphical representation of the failed scan chains. In fact, Smith questions the value of generating failing scan chains without translating into X-Y physical coordinates as stated in column 2, lines 53 - 59:

> "Scan testing enables a list of failing signals to be identified. However, even after a list of failing signals is produced for a given die, it is still not possible to find the physical location of the failure because each failing signal may contain hundreds of transistors within its "cone of logic", and there are usually multiple failing signals.

Another important part of the Smith disclosure is the express discussion to distinguish the fundamentally different concepts of "scan chains" as opposed to "netlist nodes". Smith's explanation of a "scan chain" is a discrete chain of logic which can be tested individually for basic functionality (col. 2, lines 51-53). Conversely, he defines a "netlist" as a list of low-level design cells and the interconnections between them (col. 1, lines 22-24). This is an important point that will be further discussed below.

The teachings of Testa describe a way of generating conventional ATE patterns for testing integrated circuits. Testa has no relevance whatsoever to the field of design-for-test (DFT) automatic test equipment (ATE). Additionally, Testa has no

relevance to failure diagnosis. In fact, Testa teaches pattern generation, the opposite of diagnosis. Further, Testa does not describe any form of graphical user interface (GUI), but rather a mere reference to the display of results from the testing of the device (col. 2, lines 34-35).

A) Group I Analysis

The claims of Group I distinguish over the combination of Smith and Testa by reciting a graphical user interface generator for generating graphical representations of failed scan chains. Here, the Examiner admitted that "The only limitations not recited by Smith are the use of a Graphical User Interface (GUI) or other graphical means of displaying the results." (Office Action dated 3/22/2004, page 3, para. 6). However, the examiner supplemented the disclosure of Smith by alleging that Testa discloses a GUI for use with ATE.

It is well settled that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

As noted above, there is a reason why Smith fails to make any effort to show graphical representations of scan chains - the disclosure alleges that scan chain data has little value by itself in trying to pinpoint X-Y physical locations. In other words, Smith teaches against what the invention is trying to accomplish - focus on scan chains early in the process and provide a readily comprehensible ***graphical representation*** of the failing scan chains.

Because Smith teaches against the use of the invention, there is no motivating whatsoever to import the alleged teachings of Testa to arrive at the claimed invention. As a result, the claims of Group I are nonobvious.

B) Group II Analysis

130 The claims of Group II distinguish over the combination of Smith and Testa by reciting method steps that comprise the step "**graphically displaying** a portion of the **scan chains** including the captured failure data". While much of the

Examiner's argument with respect to the claims of Group I applies, also asserted is the notion that failed netlist nodes are the same entities as failed scan chains (Office Action dated , page 4, lines 4 - 7).

As noted earlier, Smith goes to great length to explain the differences between scan chains (representing regions of logic) and netlist nodes (transistor-level connections). Applicant admits that Smith teaches how to identify and display the X-Y physical coordinates of a failed netlist node. However, as described above, this is fundamentally different than graphically displaying scan chains.

For the reasons explained above, the claims of Group II are patentable over the cited art.

2. **Conclusion**

The rejections to the claims of Groups I and II are unsupported by the cited art. Smith's teachings would not serve as motivation to combine with the teachings of Testa, nor would the combined teachings of Smith and Testa render the claimed invention obvious.

Respectfully Submitted,

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APPENDIX
Claims On Appeal

24. A DFT result diagnosis system including:

an ATE data source for providing test data in the ATE domain;

an ATPG tool operative to generate ATPG pattern data and ATPG results data in the ATPG domain;

at least one translation module to automatically convert data between multiple domains;

at least one function module to automatically summarize data from one or more devices or tests in one or more domains;

a graphical user interface generator for receiving data identifying failed scan chains and scan cells from the ATE data source and ATPG tool and generating graphical representations of the failed scan chains and cells; and

a display device coupled to receive the graphical representations from the graphical user interface, the display device operative to display the graphical representations of the failed scan chains.

25. A DFT result diagnosis system according to claim 24 wherein:

the ATE data source comprises a semiconductor tester.

26. A DFT result diagnosis system according to claim 24 wherein:

the ATE data source comprises a data repository.

27. A DFT result diagnosis system according to claim 24 wherein the at least one translation module includes:

a pattern translator to convert ATPG pattern data into ATE pattern data;

a result translator to convert ATE output data into ATPG/diagnosis tool input data; and

a mapping generator for correlating the pattern data and the results data between the ATPG/scan and the ATE domains.

32. A DFT result diagnosis system including:

a test and diagnosis engine including a semiconductor tester and a scan diagnosis tool;

a graphical user interface generator for receiving failure scan chain data identifying failed scan chains from the test and diagnosis engine and generating graphical representations of the failed scan chains; and

a display device coupled to receive the graphical representations from the graphical user interface, the display device operative to display the graphical representations of the failed scan chains.

33. A DFT result diagnosis system according to claim 32 and further including:

at least one translation module to automatically convert data between multiple domains; and

at least one function module to automatically summarize data for one or more devices or tests in one or more domains.

34. A DFT result diagnosis system according to claim 33 wherein the at least one translation module includes:

a pattern translator to convert ATPG pattern data into ATE pattern data;

a result translator to convert ATE output data into ATPG/diagnosis tool input data; and

a mapping generator for correlating the pattern data and the failure data between the ATPG/scan and the ATE domains.

35. A DFT result diagnosis system including:

means for generating pattern signals in an ATE domain to test a device-under-test and producing test output data in the ATE domain;

means for generating ATPG pattern data and ATPG results data in an ATPG domain;

means for automatically converting data between multiple domains;

means for automatically accumulating data for one or more devices or tests in one or more domains; and

means for graphically displaying the failed scan chain data.

37. A computer-readable medium having stored thereon sequences of instructions which, when executed, cause one or more electronic systems to:

capture scan failure data associated with failed scan chains from a data source;

graphically display a portion of the scan chains including the captured failure data; and

diagnose the scan failure data with a diagnosis tool.

38. A method comprising:

capturing scan failure data associated with failed scan chains from a data source;

graphically displaying a portion of the scan chains including the captured failure data; and

diagnosing the scan failure data with a diagnosis tool to produce diagnosis results data.

39. A method according to claim 38 wherein the capturing step includes:

testing a device-under-test with test pattern data in a scan format, the data source comprising the device-under-test.

40. A method according to claim 39 wherein the step of testing includes the step:

directly communicating with the diagnosis tool.

41. A method according to claim 39 wherein the step of testing includes the step:

directly communicating with the data source.

42. A method according to claim 39 wherein the step of testing includes the step:

generating ATPG pattern data in the ATPG domain with the diagnosis tool; and

automatically translating the ATPG pattern data into ATE test pattern data.

43. A method according to claim 39 wherein the step of capturing includes the step:

accumulating multiple sets of scan failure data.

44. A method according to claim 39 wherein the step of displaying includes:

displaying textual/tabular scan fail data.